JC535 U.S. PTO
04/14/98

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Ravi Iyer	Group Art Unit:	1104
Prior Application Serial No.: 08/599,675		
Prior Application Filed: February 12, 1996	Examiner:	Whipple, M.
Serial No.: Unassigned		
Filed: Herewith	Atty Docket:	MICS:0015--2/FLE 93-118.02
For: PLANARIZATION USING PLASMA OXIDIZED AMORPHOUS SILICON		

"EXPRESS MAIL" MAILING LABEL	
NUMBER:	**EL 065 999 665 US**
DATE OF DEPOSIT.	**April 14, 1998**

Pursuant to 37 C.F.R. § 1.10, I hereby certify that I am personally depositing this paper or fee with the U.S. Postal Service, "Express Mail Post Office to Addressee" service on the date indicated above in a sealed envelope (a) having the above-numbered Express Mail label and sufficient postage affixed, and (b) addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

April 14, 1998 — *Date*

Cynthia L. Hayden

Assistant Commisioner
For Patents
Washington, D.C. 20231

Dear Sir:

REQUEST FOR FILING CONTINUING APPLICATION UNDER 37 C.F.R. § 1.53(b)

This is a Request for filing a continuing application under 37 C.F.R. § 1.53(b) of pending prior application Serial No. **08/599,675**, filed on **02/12/96**, entitled **PLANARIZATION USING PLASMA OXIDIZED AMORPHOUS SILICON** in the name of **Ravi Iyer.**

The following are enclosed:

1. ___X___ Papers which the undersigned declares to be a true copy of the prior application as originally filed, including a 15 page disclosure, 2 pages of claims, a 1 page abstract of the disclosure, 2 sheets of formal drawings, and a Declaration signed by the inventor.

2. ___X___ The Commissioner is authorized to charge the filing fee as calculated below, less any claims canceled by amendment below, and any additional fees which may be required, to Deposit Account No. 13-3092, Order No. MICS:0015--2/FLE (93-118.02).

3.a. ___X___ A copy of the Election and Power of Attorney in the prior application.

or

3.b. _____ A new Power of Attorney.

4. ___X___ An Assignment of record for the prior application.

5. ___X___ Three (3) sets of formal drawings, each set consisting of 2 sheets.

6.a. _____ A verified statement claiming small entity status is enclosed.

or

6.b. _____ A verified statement claiming small entity status was filed in a parent application and small entity status is still proper and desired in this continuing application.

7. __X__ An Information Disclosure Statement and PTO-1449.

9. __X__ Preliminary Amendment.

__X__ Please address all correspondence in connection with this application to **Michael G. Fletcher, Fletcher, Yoder & Edwards, P.O. Box 692289, Houston, Texas 77269-2289; telephone (281) 970-4545.**

__X__ Amend the specification by inserting before the first line the sentence:

--This application is a Continuation of application Serial No. 08/599,675 filed 02/12/96.--

__X__ Cancel in this application original claims 2-11 of the prior application before calculating the filing fee. (At least one original independent claim must be retained for filing purposes.)

The filing fee is calculated on the basis of the claims originally filed in the prior application, and any claims canceled or added by amendment.

CLAIMS	FOR	NUMBER FILED	NUMBER EXTRA	RATE	CALCULATIONS
	TOTAL CLAIMS 13	- 20 =	0	X $ 22 00	$
	INDEPENDENT CLAIMS 3	- 3 =	0	X $ 82.00	
	MULTIPLE DEPENDENT CLAIM(S) (If applicable)			+ 270.00	
				BASIC FEE	790.00
			Total of above Calculations =		790.00
	Reduction by ½ for filing by small entity (Note 37 C.F.R §§ 1.9, 1.27. 1.28.				$
				TOTAL =	$ 790.00

The undersigned declares that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: April 14, 1998

Michael G. Fletcher
Reg. No. 32,777
Fletcher, Yoder & Edwards
P.O. Box 692289
Houston, Texas 77269-2289
(281) 970-4545

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April 14, 1998 (Date) — Cynthia L. Hayden

Assistant Commisioner
For Patents
Washington, D.C. 20231

Dear Sir:

PRELEMINARY AMENDMENT

Prior to examination of the above-referenced application, please amend the application as follows:

IN THE CLAIMS

Please cancel claims 2-11 without prejudice.

Please add new claims 12-23 as set forth below:

12 (new). A method of manufacturing an integrated circuit, the method comprising the steps of:

(a) forming features on a substrate, the features protruding from the substrate to create creases adjacent the features;

(b) depositing a layer of non-dielectric material over the features and the creases;

(c) removing a portion of the layer of non-dielectric material, leaving stringers of the non-dielectric material in the creases; and

(d) converting the stringers of non-dielectric material in the creases into a dielectric material.

13 (new). The method, as set forth in claim 12, wherein step (a) comprises the step of forming gate electrodes protruding from the substrate.

14 (new). The method, as set forth in claim 12, wherein step (b) comprises the step of depositing a layer of silicon over the features and the creases.

15 (new). The method, as set forth in claim 12, wherein step (c) comprises the step of etching the portion of the layer of non-dielectric material.

16 (new). The method, as set forth in claim 12, wherein step (d) comprises the step of oxidizing the stringers.

17 (new). The method, as set forth in claim 12, wherein step (d) comprises the step of nitridizing the stringers.

18 (new). A method of manufacturing an integrated circuit, the method comprising the steps of:

(a) forming features on a substrate, the features protruding from the substrate to create creases adjacent the features;

(b) depositing a layer of non-dielectric material over the features and the creases;

(c) removing a portion of the non-dielectric material from the creases using a given method, the given method leaving residual non-dielectric material in some of the creases; and

(d) converting the residual non-dielectric material in the creases into a dielectric material.

19 (new). The method, as set forth in claim 18, wherein step (a) comprises the step of forming gate electrodes protruding from the substrate.

20 (new). The method, as set forth in claim 18, wherein step (b) comprises the step of depositing a layer of silicon over the features and the creases.

21 (new). The method, as set forth in claim 18, wherein the given method comprises an etching method.

22 (new). The method, as set forth in claim 18, wherein step (d) comprises the step of oxidizing the residual non-dielectric material.

23 (new). The method, as set forth in claim 18, wherein step (d) comprises the step of nitridizing the residual non-dielectric material.

REMARKS

Claims 2-11 have been canceled without prejudice, and new claims 12-23 have been added. Consideration of the application as amended is respectfully requested.

If the Examiner believes that a telephonic interview will help speed this application toward issuance, Applicant invites the Examiner to contact the undersigned at (281) 970-4545.

Respectfully submitted,

Date: April 14, 1998

Michael G. Fletcher
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(281) 970-4545

09059865.041498

PLANARIZATION USING PLASMA OXIDIZED AMORPHOUS SILICON

BACKGROUND OF THE INVENTION

1. Field of the Invention.

The present invention relates, in general, to planarization methods and, more particularly, to a method and apparatus for filling gaps between metal lines in multilayer metallization structures.

2. Statement of the Problem.

Integrated circuit technology has advanced through continuing improvements in photolithographic processing so that smaller and smaller features can be patterned onto the surface of the substrate. Spaces or gaps exist between these patterned features. Integrated circuit surfaces also contain trench or via structures protruding down into the surface. The lateral dimensions of such structures is hereinafter referred to as the width of the gap trench or via: the vertical dimension of such structures is referred to as the depth. The

aspect ratio is the ratio of the depth to width. The smaller features, with smaller spaces between features, result in high aspect ratio gaps, trenches and vias. These high aspect ratio structures must be filled with an appropriate material before continued processing. This problem is acute in the case of multilayer metal (MLM) designs. In MLM designs each metal layer must be planarized by filling the gaps between metal features with dielectric before a subsequent metal layer can be formed and patterned.

When a deposited film is used to completely fill the high aspect ratio structure three different results can emerge. In one case, the deposited material fills the trench without leaving a seam or void. In a second case, a seam arises from the point where the sidewall layers merge during deposition. In a third case, a void arises if the deposition produces re-entrant profiles at earlier stages of the filling process. The first creates the highest reliability integrated circuits. The seams and voids are undesirable because chemicals or materials may be present in the seam or void to corrode or degrade the structure. Further, voids are rarely hermetically sealed, so subsequent exposure to chemicals or materials deposition can alter the material structure substantially.

Deposition onto patterned features is practiced at several stages and fabrication of semiconductor devices in integrated circuits. Most often the objective is to provide a highly conformal film or a void-free fill. Low pressure chemical vapor deposition (LPCVD) and plasma enhanced chemical vapor deposition (PECVD) are widely used to provide conformal deposition of thin films over three dimensional features. A number of CVD films are currently used in various steps in processing. Typically, sidewall coverage is not uniform along the height of a trench or a via. Low temperature plasma-enhanced deposition and etching techniques are used to form diverse materials including dielectric films such as silicon nitride and silicon dioxide and semiconductor films such as amorphous and polycrystalline silicon. The plasma used in the plasma-enhanced CVD process is a low pressure plasma that is developed in a radio frequency (RF) field. The RF plasma results in a very high electron temperature making possible the deposition of dense, good quality films at lower temperatures and faster deposition rates than are typically possible using purely thermally activated CVD processes.

Current CVD processes have important limitations. With high integration levels, higher aspect ratios are required, stretching the ability of known CVD processes. Seams and voids

all endanger the manufacturability of semiconductor product due to the yield and reliability problems they present. Where higher growth temperatures improve conformality or profiles, other properties of the three dimensional structure may be degraded (i.e. abrupt doping profiles due to diffusion). Further, higher growth temperatures cannot be used after metallization.

Planarization processes are particularly difficult after metallization is applied to an integrated circuit. All processes subsequent to metal deposition must be performed at sufficiently low temperature such that the metal does not melt or vaporize. Conventionally this has limited post metallization processing to thin film deposition together with patterning or polishing those thin films. Oxidation processes are almost entirely unused after metal deposition.

Step coverage and filling of high aspect ratio gaps with CVD films is a continuing problem in the integrated circuit manufacturing industry. Decreasing costs for most IC products forces increasingly efficient production and higher throughput of film deposition processes. What is needed is a method and apparatus for highly conformal CVD deposition and planarization after deposit and patterning of metal films.

Other prior art planarization processes include deposit-etch-deposit processes whereby a thin film of an insulating material is deposited then etched or polished from the surface to mechanically planarize the film followed by subsequent deposit and etch processes until a planar surface is achieved. As metal line pitch is reduced, the deposit-etch-deposit processes leave voids between the metal lines that cannot be filled.

Another prior process is spin on glass (SOG) planarization. SOG uses a suspension of glass particles in an organic carrier that can be spun onto a wafer in a thin film using conventional photoresist tools. The organic carrier is then driven off in thermal processing and the glass reflowed to fill spaces between metal lines. Spin on glass planarization is plagued with via poisoning caused by contaminants in the spin on glass and the organic carrier that cannot adequately be removed during subsequent processing.

U.S. Patent 5,182,221 issued to Sato on January 26, 1993 describes an ECR-CVD process in which etching and deposition are simultaneously performed. In one embodiment, the Sato deposition process is performed in a single step with carefully controlled conditions to provide a ratio of vertical to horizontal deposition rate that will fill high aspect ratio trenches. The

Sato process provides high quality via fill at the cost of increased control and reduced deposition rates. Further, because of high equipment costs associated with the ECR-CVD processes, they have limited applicability and are not heavily used in IC manufacturing.

A need exists for a process for filling spaces between pattern metallization features with dielectric using existing equipment technology that provides high quality void free via filling.

3. Solution to the Problem.

The above identified problems and others are solved by a planarization method using a thin film of expandable material applied to a surface of patterned metal features. The expandable material is treated at low temperature to cause a volume increase and fill the spaces between metal features. In this manner the spaces between metal features are filled in a void-free, seam free-manner at temperatures well below the melting point of the metal features.

SUMMARY OF THE INVENTION

Briefly stated, the present invention involves a planarization process for filling spaces between patterned metal features formed over a surface of a semiconductor substrate. The patterned metal features are preferably coated with a dielectric barrier. The dielectric barrier is coated with an oxidizable material such as silicon to a thickness about half the depth of the space between metallized features. The oxidizable layer is then plasma oxidized using an RF or ECR plasma at low temperature with an oxygen or ozone ambient. Alternatively, a material that expands during nitridization is substituted for the oxidizable material and the step of plasma oxidation is replaced by a step of plasma nitridization. The plasma oxidation or nitridization is continued until the expandable material is converted to a dielectric and has expanded to fill the space between patterned metal features. Optionally, the process can be followed by a mechanical or chemical mechanical planarization step.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 illustrates a semiconductor wafer having patterned metallized features formed thereon;

FIG. 2 illustrates the process in accordance with the present invention at an early stage of processing;

FIG. 3 illustrates the process in accordance with the present invention after further processing;

FIG. 4 illustrates the semiconductor substrate shown in FIG. 3 at a further stage in processing;

FIG. 5 illustrates the substrate shown in FIG. 4 at a later stage in planarization;

FIG. 6 shows a second embodiment of the method of the present invention;

FIG. 7 illustrates the second embodiment of FIG. 6 at a later stage of processing; and

FIG. 8 shows the second embodiment after completion of the process in accordance with the present invention.

DETAILED DESCRIPTION OF THE DRAWING

The present invention involves a method of filling spaces between patterned metal features on a semiconductor substrate with dielectric material. While the preferred embodiment is described in terms of metal lines formed directly on a semiconductor substrate, it will be apparent to those with skill in semiconductor processing that the patterned metal features in accordance with the present invention can be formed on a semiconducting, insulating, or conductive substrate. Similarly, the substrate may comprise one or more layers of semiconductor, conductor, or insulator material with electronic devices fabricated in one or more of the layers. While the present invention is particularly adapted to high aspect ratio patterned metal features, the present invention may be employed in any metallization scheme.

In order to form a dielectric layer between metal features, it is necessary to perform all processing at temperatures below the melting point of the metal. It is desirable to perform the processes well below the melting temperature in order to avoid diffusion of the metal into surrounding materials.

FIG. 1 illustrates a substrate 101 which is preferably a semiconductor material but may comprise a single layer, or multilayer integrated circuit device. Typically, devices would be

fabricated in substrate 101 and a metallization 102 provided to make electrical contact to the semiconductor devices. However, for ease of description semiconductor devices are not illustrated in substrate 101. The structures shown in FIG. 1 are not drawn to scale: a moderate aspect ratio structure is shown having an aspect ratio of about 1:1. The present invention is particularly useful in higher aspect ratio structures.

As shown in FIG. 2, metallized features and exposed portions of substrate 101 are conformally coated with an insulating layer 201. Insulating layer 201 may be silicon dioxide or silicon nitride or similar insulating material that serves as a barrier between metal 102, substrate 101, and any subsequent materials deposited. Insulating layer 201 can be applied by conventional low pressure chemical vapor deposition (LPCVD) or plasma enhanced chemical vapor deposition (PECVD). CVD processes are known to provide conformal coating of delicate high aspect ratio features and so are preferable to other methods of thin film formation.

As shown on FIG. 3, insulating layer 201 is preferably facet etched in accordance with the method of the present invention. Facet etching is accomplished in a plasma reactor using well known processes. As can be seen by comparing FIG. 2 and FIG. 3, the facet etch step results in

an overall thinning of insulating layer 201 as well as faceted edges in insulating layer 201 over corners of metal features 102. Faceted edges are easier to cover by subsequent deposition steps.

In FIG. 4, an oxidizable layer 401 is conformally deposited preferably using a CVD process. Oxidizable layer 401 comprises a material that expands during oxidation such as amorphous silicon. Polycrystalline silicon also could be used, but require higher deposition temperatures and affords little advantage over amorphous silicon. Any material that can be treated at low temperature to expand into an insulating fill material is an acceptable equivalent to the amorphous silicon used in oxidizable layer 401 of the preferred embodiment.

The thickness of oxidizable layer 401 is determined from the amount of expansion possible when oxidizable layer 401 is subsequently treated. In the preferred embodiment where oxidizable layer 401 comprises amorphous silicon, layer 401 should be about 50% of the total distance between patterned metal features 102. This is because the amorphous silicon will expand or swell to about two times its original volume once converted to SiO_2. Because a relatively thin layer is used (i.e., 0.15 micron to fill a 0.3 micron space), there is little problem with voids

or seams during the deposition of oxidizable layer 401.

FIG. 5 illustrates a substrate at a later stage in processing. The substrate shown in FIG. 4 including oxidizable layer 401 are exposed to a plasma oxidation process. Plasma oxidation is a low temperature, high radio frequency power method of silicon oxidation used to form silicon dioxide films. Alternatively, electron cyclotron resonance (ECR) plasma processing can be used. Preferably, the plasma reactor includes magnetron electrodes to increase the power density of the plasma. Substrate temperature can be maintained below 300 degrees C and preferably below 150 degrees C. Significantly, the plasma oxidation process is not a deposition process and requires only an oxygen ambient to react with the oxidizable layer 401. Because no deposition occurs, oxidizable layer 401 expands or swells to almost twice its volume during the oxidation process and does not create seams or voids between metal features 102.

Optionally, the substrate shown in FIG. 5 after the plasma oxidation process can be mechanically or chemical mechanically polished to further planarize the surface using known planarization techniques in combination with the method of the present invention. Because the filling between metal features 102 is

substantially void and seam free, the chemical mechanical polish produces superior results.

A more general application of the method in accordance with the present invention is shown in FIG. 6 through FIG. 8. In this embodiment, the present invention is used to tailor surface contours but unlike the first embodiment, planarization is not the end goal. In FIG. 6, device features 601 protrude from the surface of substrate 101. In the case of FIG. 6, device features 601 comprise multiple layers of insulator and conductor used to form a gate electrode structure in a MOSFET process. The specific composition and layer arrangement are not important for the present invention so long as it is understood that protruding device features 601 may comprise one or more layers of insulator, conductor, refractory metal silicide, semiconductor, or equivalent material.

Many semiconductor processes involve forming a blanket deposited layer 602 over protruding device features 601. In particular, polysilicon or amorphous silicon are commonly used to form capacitor structures or device contacts. As shown in FIG. 7, layer 602 is patterned and etched to clear areas where layer 602 is not needed. This is done, for example, to expose source and drain regions on either side of a gate electrode. The removal process, however, often leave "stringers" 701 as a residue that are

difficult to remove without damaging the structure or topology of protruding features 601.

Where layer 602 comprises an material that is expandable in a plasma oxidation or nitridization process, the present invention can be used to protect the topology and structure of protruding feature 601 by contouring (without planarizing) the protruding feature. In this embodiment, the structure shown in FIG. 7 is exposed to the plasma oxidation or nitridization process to convert stringers 701 to an insulating material such as sidewalls 801 shown in FIG. 8. Because low temperature plasma oxidation is used, the present invention provides the desirable contour with minimal impact on the thermal budget for various other device features. In the specific example of a gate electrode with polysilicon stringers, the stringer 701 causes gate leakage whereas the sidewall 801 both protects the gate electrode from undercutting and provides a better contour for further processing.

By now it is appreciated that a method for filling gaps between patterned device features with insulating material is provided. Using a deposited thin film of an expandable material allows the thin film to be conformally deposited onto the patterned metal features without voids or seams. A low temperature plasma oxidation converts the deposited layer into an insulating layer and causes it to increase in volume sufficiently to fill the gap between metal

features. It is to be expressly understood that the claimed invention is not to be limited to the description of the preferred embodiment but encompasses other modifications and alterations within the scope and spirit of the inventive concept.

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WE CLAIM:

1. A method for filling spaces between patterned metal features, the method comprising the steps of:

coating the patterned metal features with a first material so as to partially fill the space between the metal features; and

treating the first material at a temperature less than a melting point of the metal features so as to cause the first material to expand.

2. The method of claim 1 wherein the coating step comprises CVD process.

3. The method of claim 1 wherein the coating step comprises deposition of amorphous silicon.

4. The method of claim 1 further comprising depositing an insulating barrier layer on the patterned metal features before the step of coating.

5. The method of claim 4 further comprising the step of facet etching the insulating barrier layer before the step of coating.

6. The method of claim 1 wherein the step of treating comprises plasma oxidation.

7. The method of claim 1 wherein the step of treating comprises plasma nitridization.

8. A method for manufacturing a semiconductor device comprising the steps of:

providing a semiconductor substrate;

forming patterned features protruding from a surface of the substrate, wherein recessed areas exist between the protruding features;

forming a material capable of expansion upon further reaction on the protruding features;

reacting the material capable of expansion to cause it to expand so as to contour the protruding features.

9. The method of claim 8 wherein the protruding features are gate electrodes, the material capable of expansion comprises silicon, and the step of forming comprises blanket deposition followed by an etch leaving silicon stringers on the protruding features.

10. The method of claim 9 wherein the step of reacting comprises plasma oxidation.

11. The method of claim 9 wherein the step of reacting comprises plasma nitridization.

ABSTRACT OF THE DISCLOSURE

A planarization process for filling spaces between patterned metal features formed over a surface of a semiconductor substrate. The patterned metal features are preferably coated with a dielectric barrier. The dielectric barrier is coated with an material that expands during oxidation or nitridization to a thickness about half the depth of the space between metallized features. The layer is then plasma oxidized using an RF or ECR plasma at low temperature with an oxygen ambient. Alternatively, the layer is plasma nitridized at low temperature. The plasma oxidation or nitridization is continued until the expandable material is converted to a dielectric and has expanded to fill the space between patterned metal features. Optionally, the process can be followed by a mechanical or chemical mechanical planarization step.

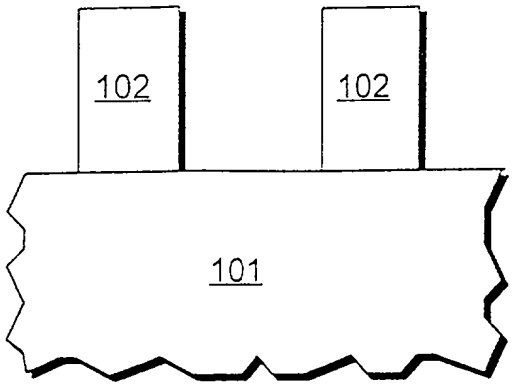

FIG. 1

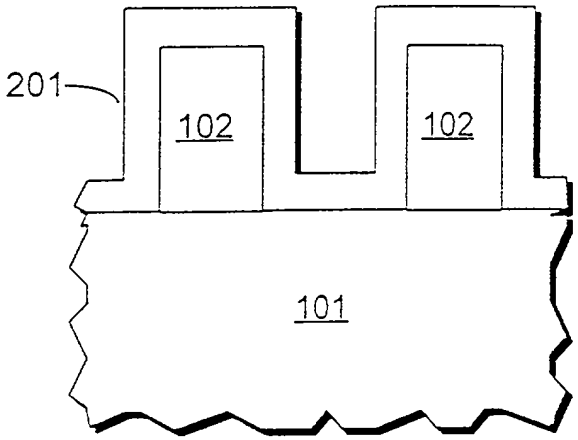

FIG. 2

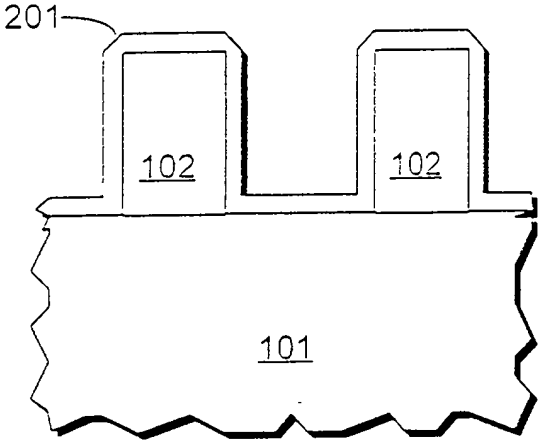

FIG. 3

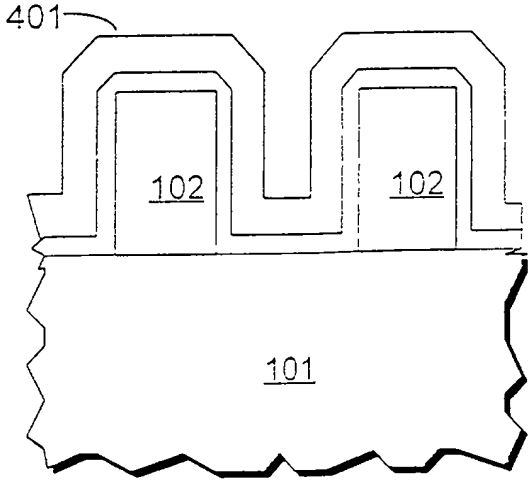

FIG. 4

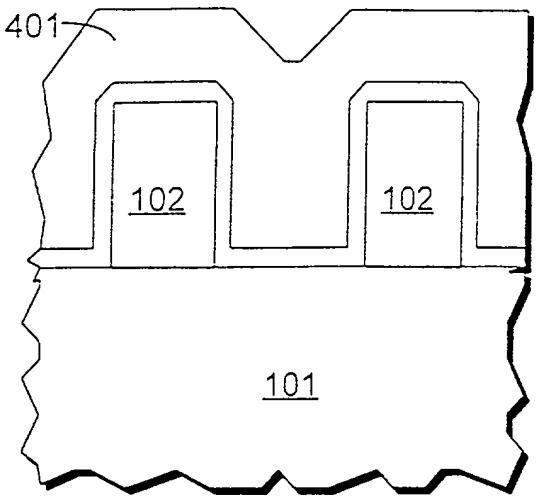

FIG. 5

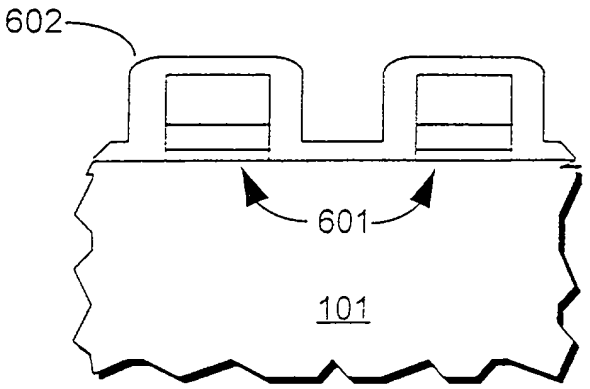

FIG. 6

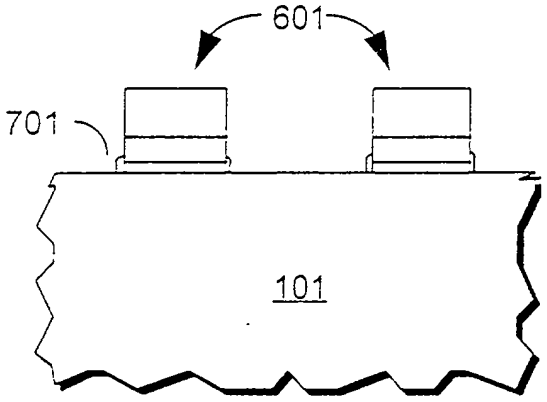

FIG. 7

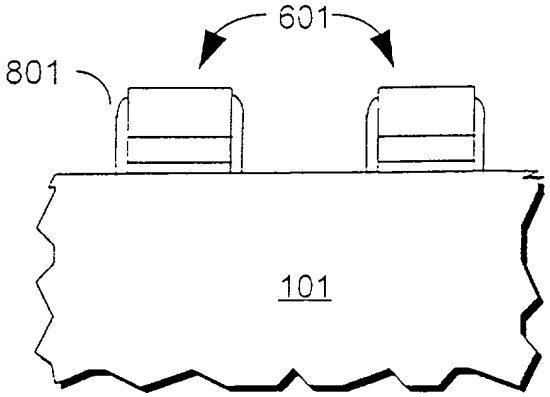

FIG. 8

DECLA ‹TION FOR PATENT APPLICA› ›N

Docket No. (Optional)
1402/26

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:
THE USE OF PLASMA OXIDIZED A-SI TO FILL SPACES INBETWEEN METAL LINES AND PLANARIZATION, the specification of which is attached hereto unless the following box is checked:

☐ was filed on _____ as United States Application Number or PCT International Application Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.
I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.
I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes ☒ No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	(Filing Date)	(Status-patented, pending, abandoned)
(Application Number)	(Filing Date)	(Status-patented, pending, abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: Robert C. Dorr 27,782; W. Scott Carson 27,292; Jack C. Sloan 26,806; Thomas S. Birney 30,025; Stuart T. Langley 33,940; Brian A. Carpenter 37,109; and Leslie P. Kramer 38,521;

Address all telephone calls to Stuart T. Langley at telephone no. (303) 333-3010
Address all correspondence to Dorr, Carson, Sloan & Birney, P.C.
3010 E. 6th Avenue,
Denver, Colorado 80206

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor (given name, family name): Ravi Iyer

Inventor's signature: Ravi Iyer Date: 2/7/96
Residence: Boise, Idaho Citizenship: India
Post Office Address: 5600 South Fuchsia Place
Boise, Idaho 83705

Full name of second joint inventor if any (given name, family name): _____

Inventor's signature: _____ Date: _____
Residence: _____ Citizenship: U.S.A.
Post Office Address: _____
_____

☐ Additional inventors are being named on separately numbered sheets attached hereto.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	§	
	§	
Ravi Iyer	§	Group Art Unit: 1109
	§	
Serial No.: 08/599,675	§	
	§	Examiner: Unassigned
Filed: February 12, 1996	§	
	§	
For: PLANARIZATION USING PLASMA OXIDIZED AMORPHOUS SILICON	§	Atty Docket: MICS:0015 93-118
	§	

ELECTION UNDER 37 C.F.R. §§ 3.71 AND 3.73 AND POWER OF ATTORNEY

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The undersigned, being Assignee of the entire interest in the above-identified application by virtue of an Assignment recorded in the United States Patent and Trademark Office as set forth below, hereby elects, under 37 C.F.R. § 3.71, to prosecute the application to the exclusion of the inventor(s).

The Assignee hereby revokes any previous Powers of Attorney and appoints:

Michael L. Lynch, Reg. No. 30,871; and Lia Pappas Dennison, Reg. No. 34,095

of MICRON TECHNOLOGY, INC.; and also

Michael G. Fletcher, Reg. No. 32,777

with the law firm of FLETCHER & ASSOCIATES, P.C. as its attorneys, so long as they remain with such firms, with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the Patent and Trademark Office in connection therewith, to receive any Letters Patent, and for one year after issuance of such Letters Patent to file any request for a certificate of correction that may be deemed appropriate.

Pursuant to 37 C.F.R. § 3.73, the undersigned has reviewed the evidentiary documents, specifically the Assignment to MICRON TECHNOLOGY, INC. referenced below, and certifies that to the best of my knowledge and belief, title remains in the name of the Assignee.

Please direct all communications as follows:

Michael G. Fletcher
FLETCHER & ASSOCIATES, P.C.
P.O. Box 11850
Spring, TX 77391-1850
(281) 370-4545

ASSIGNEE: Micron Technology, Inc.

Date: 1-3-97

By: _____
Name: Michael L. Lynch, Chief Patent Counsel

ASSIGNMENT:

_____ Enclosed for recording
__X__ Previously recorded: Date: 02-12-96
Reel: 8190
Frame: 0268

RECORDED: 01/03/1997

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Ravi Iyer	)	Docket No.: 93-118 (1402/26)
	)	
Serial No.:	)	Group Art Unit:
	)	
Filed: Concurrently herewith	)	Examiner:
	)	
For: THE USE OF PLASMA OXIDIZED A-SI TO FILL SPACES INBETWEEN METAL LINES AND PLANARIZATON	)	

ASSIGNMENT:

__X__ Enclosed for recording
_____ Previously recorded
Date: _____
Reel: _____

ASSIGNMENT

FOR GOOD AND VALUABLE CONSIDERATION, the receipt, sufficiency and adequacy of which are hereby acknowledged. the undersigned, do hereby:

SELL, ASSIGN AND TRANSFER to **Micron Technology, Inc.** (the "Assignee"), a corporation of Delaware, having a place of business at 8000 South Federal Way, P.O. Box 6, Boise, Idaho 83707-0006, the entire right, title and interest for the United States and all foreign countries, in and to any and all improvements which are disclosed in the application for United States Letters Patent, which has been executed by the undersigned concurrently herewith and is entitled: **THE USE OF PLASMA OXIDIZED A-SI TO FILL SPACES INBETWEEN METAL LINES AND PLANARIZATION**; such application and all divisional, continuing, substitute, renewal, reissue and all other applications for patent which have been or shall be filed in the United States and all foreign countries on any of such improvements; all original and reissued patents which have been or shall be issued in the United States and all foreign countries on such improvements; and specifically including the right to file foreign applications under the provisions of any convention or treaty and claim priority based on such application in the United States of America;

AUTHORIZE AND REQUEST the issuing authority to issue any and all United States and foreign patents granted on such improvements to the Assignee;

WARRANT AND COVENANT that no assignment. grant, mortgage, license or other agreement affecting the rights and property herein conveyed has been or will be made to others by the undersigned, and that the full right to convey the same as herein expressed is possessed by the undersigned:

COVENANT that, when requested and at the expense of the Assignee, to carry out in good faith the intent and purpose of this assignment, the undersigned will execute all divisional, continuing, substitute, renewal, reissue, and all other patent applications on any and all such improvements; execute all rightful oaths, declarations, assignments, powers of attorney and other improvements and the history thereof; and generally do everything possible which the Assignee shall consider desirable for securing, maintaining and enforcing proper patent protection for such improvements and for vesting title to such improvements in the Assignee;

TO BE BINDING on the heirs, assigns, representatives and successors of the undersigned and extend to the successors, assigns and nominees of the Assignee.

(Signature) Ravi Iyer Date: 2/7/96

Ravi Iyer

STATE OF IDAHO)
) ss.
County of Ada)

BEFORE ME, this 7th day of February, 1996, personally appeared the above-named individual(s), to me known to be the person(s) who is (are) described in and who executed the foregoing assignment instrument and acknowledged to me that he/she (they) executed the same of his/her (their) own free will for the purpose therein expressed.

SEAL

CHRISTINA I. NORDBERG NOTARY PUBLIC STATE OF IDAHO

Christina I Nordberg
Notary or Consular Officer
My Commission Expires 9-8-2000